

## 74F158A Quad 2-Input Multiplexer

### General Description

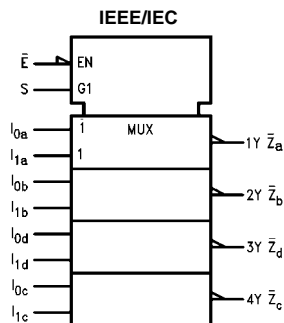
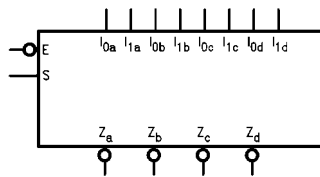
The F158A is a high speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four outputs present the selected data in the inverted form. The F158A can also generate any four of the 16 different functions of two variables.

### Ordering Code:

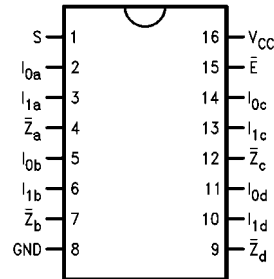
Order Number	Package Number	Package Description
74F158ASC (Note 1)	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74F158ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F158APC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

**Note 1:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



## Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$I_{0a}-I_{0d}$	Source 0 Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$I_{1a}-I_{1d}$	Source 1 Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
S	Select Input	1.0/1.0	20 $\mu$ A/-0.6 mA
$\bar{Z}_a-\bar{Z}_d$	Inverted Outputs	50/33.3	-1 mA/20 mA

## Truth Table

Inputs				Outputs
$\bar{E}$	S	$I_0$	$I_1$	$\bar{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

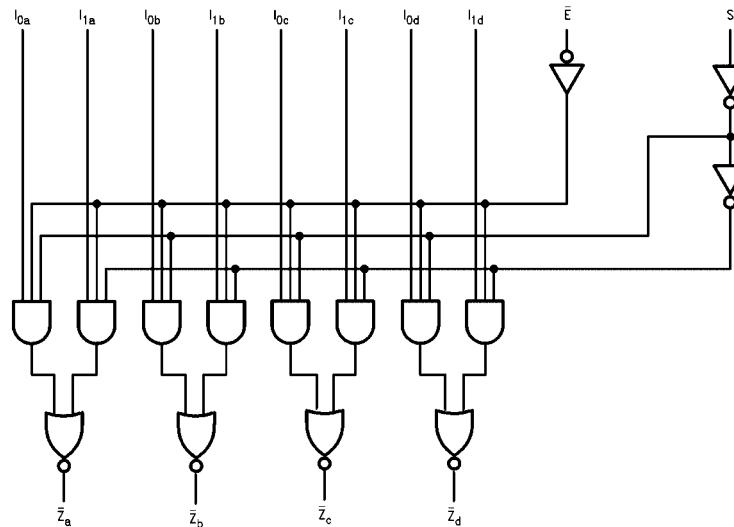
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 $\bar{Z}_n = \bar{E} \times (I_{1n}S + I_{0n}\bar{S})$

## Functional Description

The F158A quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ( $\bar{E}$ ) is active LOW. When  $\bar{E}$  is HIGH, all of the outputs ( $\bar{Z}$ ) are forced HIGH regardless of all other inputs. The F158A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

A common use of the F158A is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The F158A can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

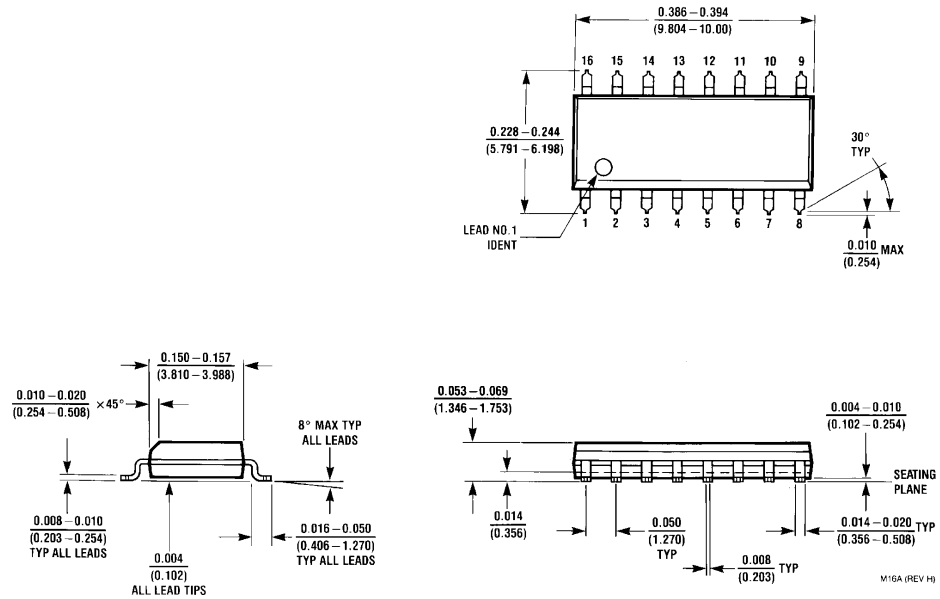
**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		10	15	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		15	25	mA	Max	V <sub>O</sub> = LOW

**AC Electrical Characteristics**

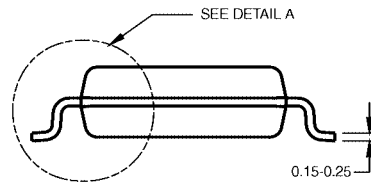
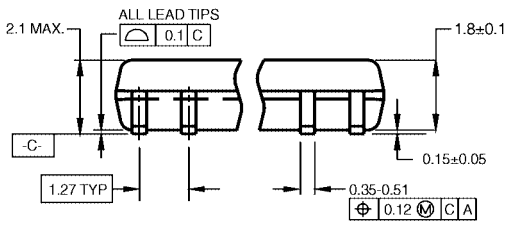
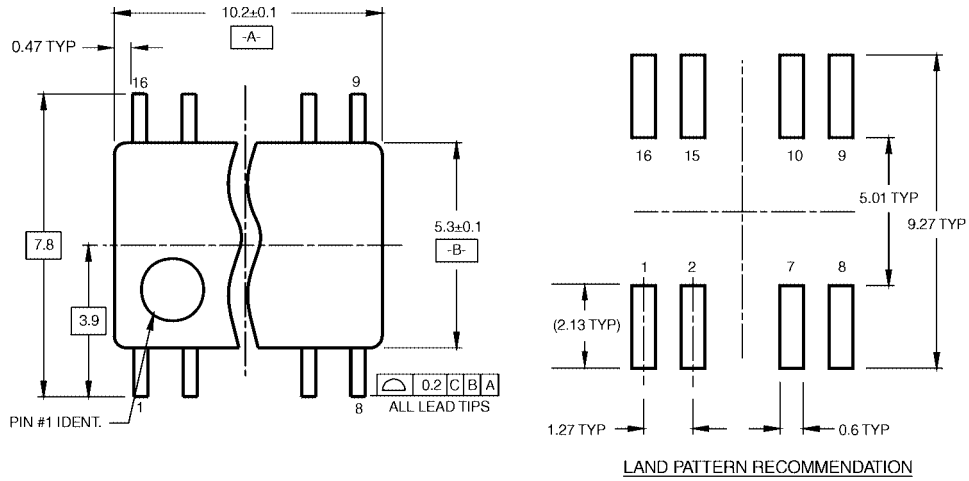
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay S to $\bar{Z}_n$	3.0	5.5	8.5	3.0	10.5	3.0	9.5	ns
t <sub>PHL</sub>	S to $\bar{Z}_n$	2.5	4.5	6.5	2.5	8.0	2.5	7.0	ns
t <sub>PLH</sub>	Propagation Delay $\bar{E}$ to $\bar{Z}_n$	2.5	4.5	6.0	2.5	8.0	2.5	7.0	ns
t <sub>PHL</sub>	$\bar{E}$ to $\bar{Z}_n$	2.0	4.0	6.0	2.0	7.0	2.0	6.5	ns
t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to $\bar{Z}_n$	2.5	4.0	5.9	2.5	8.5	2.5	7.0	ns
t <sub>PHL</sub>	I <sub>n</sub> to $\bar{Z}_n$	1.5	2.5	4.0	1.0	5.0	1.5	4.5	ns

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A**

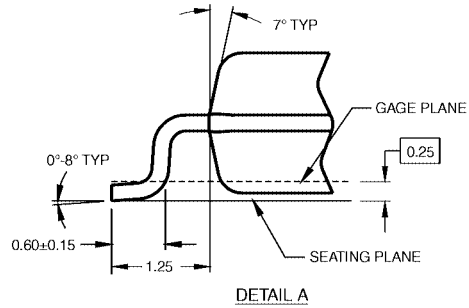
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

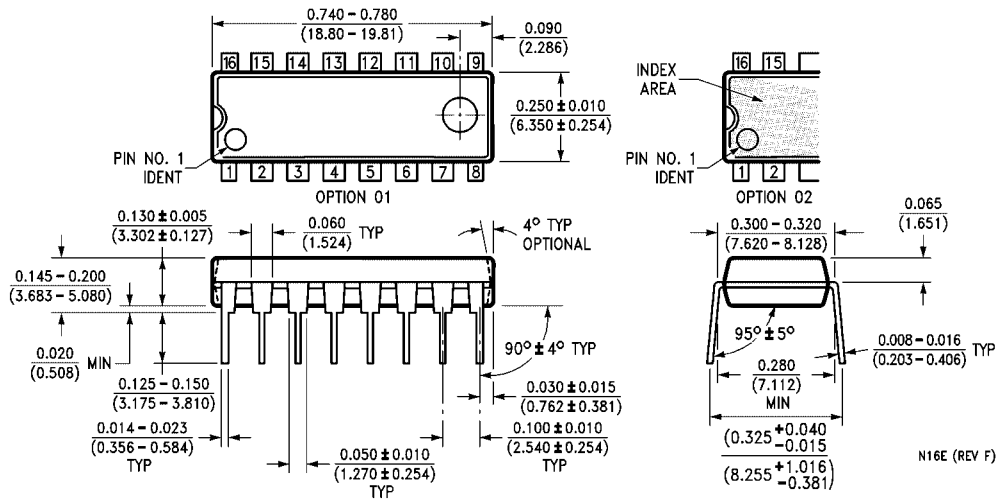
- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
 Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E**

N16E (REV F)

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